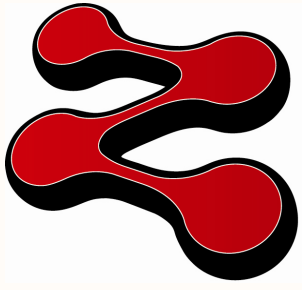
| ZedBoard | |
|---|---|
| Digilent | |
| www.zedboard.org | |
| **Function** | **Sheet Number** |
| Cover Sheet | 1 |
| FMC, AMS Connectors | 2 |
| PMODS, General I/O | 3 |
| Audio Codec | 4 |
| HDMI, VGA | 5 |
| Ethernet, OLED, SD Card | 6 |
| USB, UART | 7 |
| FPGA Configuration | 8 |
| FPGA Banks | 9 |
| DDR, MIO Banks | 10 |
| FPGA Power | 11 |
| USB Programming | 12 |
| DDR3 Memory | 13 |
| DDR Termination | 14 |
| Power Regulation | 15 |
| Power Regulation | 16 |
| Power Regulation | 17 |



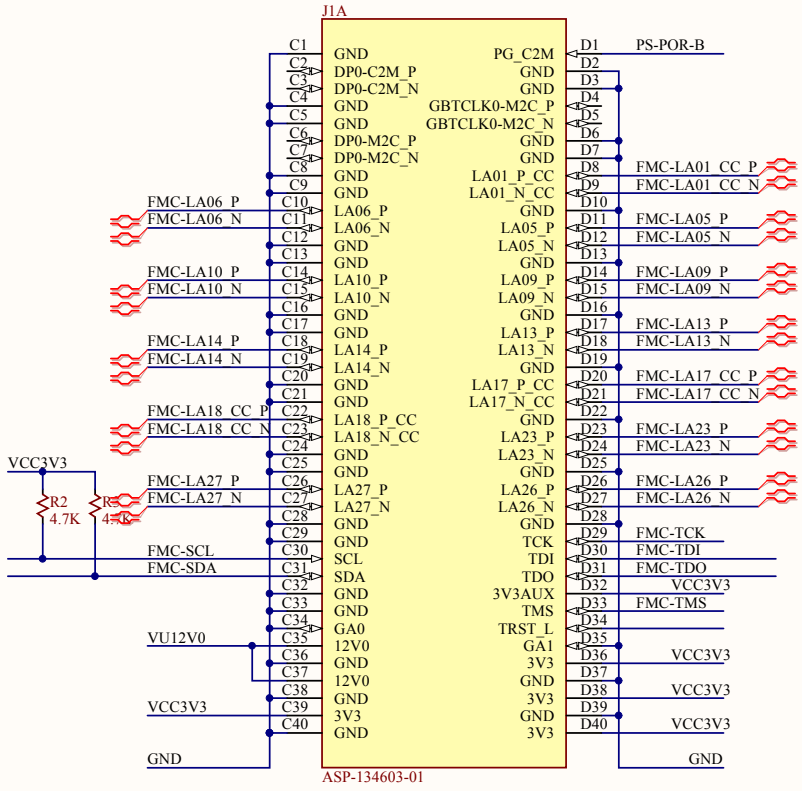
# ZedBoard

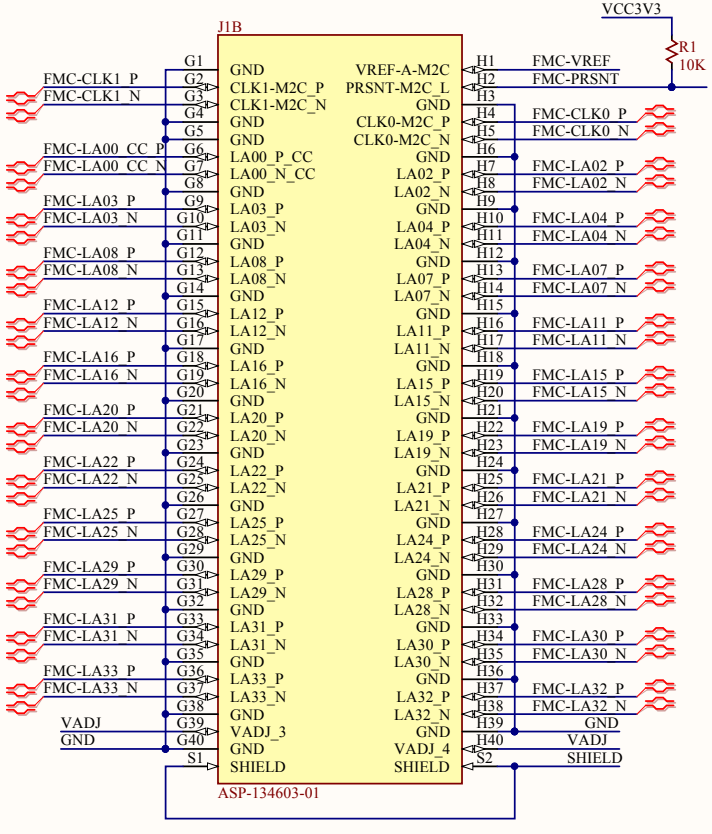
# 16 Jan 2013

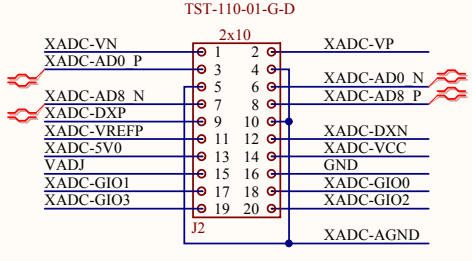


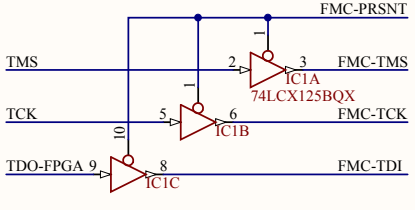
| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 1 out of 17 |

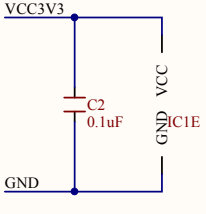
DIGILENT® BEYOND THEORY

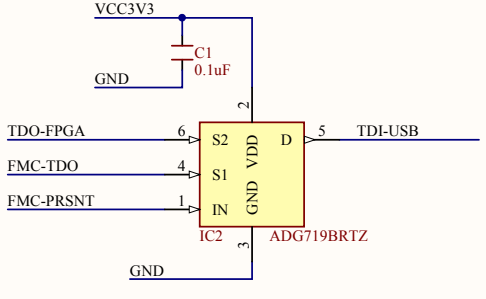


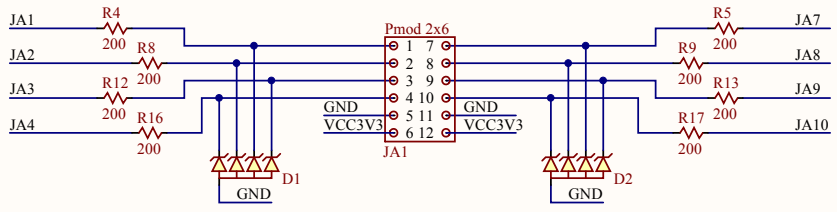

Foot F1
Foot F2
Foot F3
Foot F4

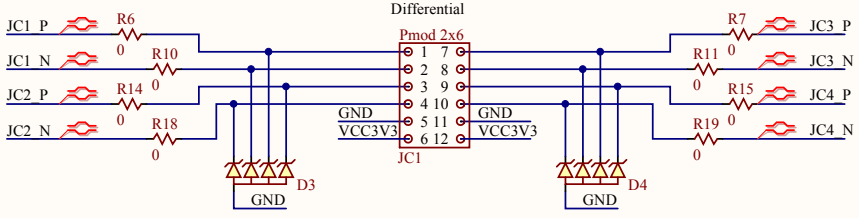
ZED Board

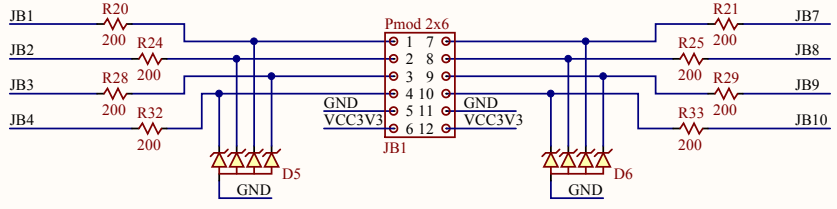
Digilent Inc. ROHS Chinese ROHS Avnet CE

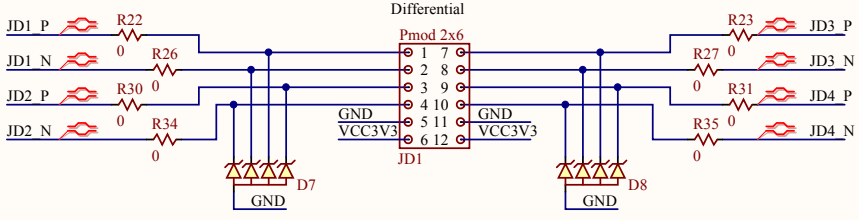
| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | FMC and AMS Connector |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 2 out of 17 |

DIGILENT BEYOND THEORY

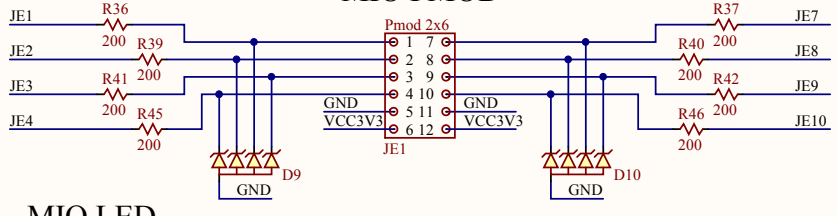


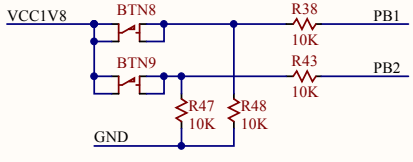



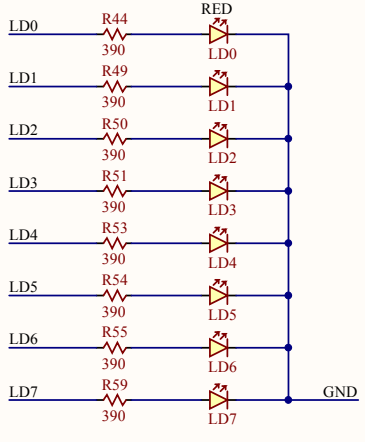




## MIO PMOD

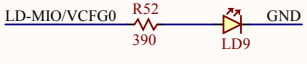


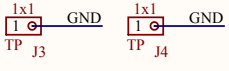

## MIO BUTTON

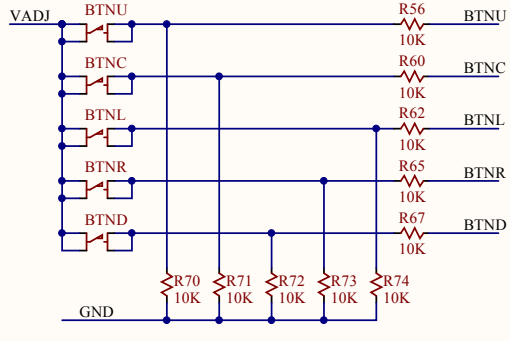


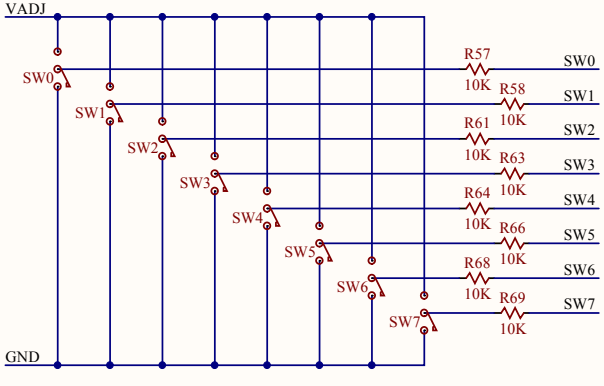




## MIO LED




| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | PMODs andGeneral I/O |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 3 out of 17 |

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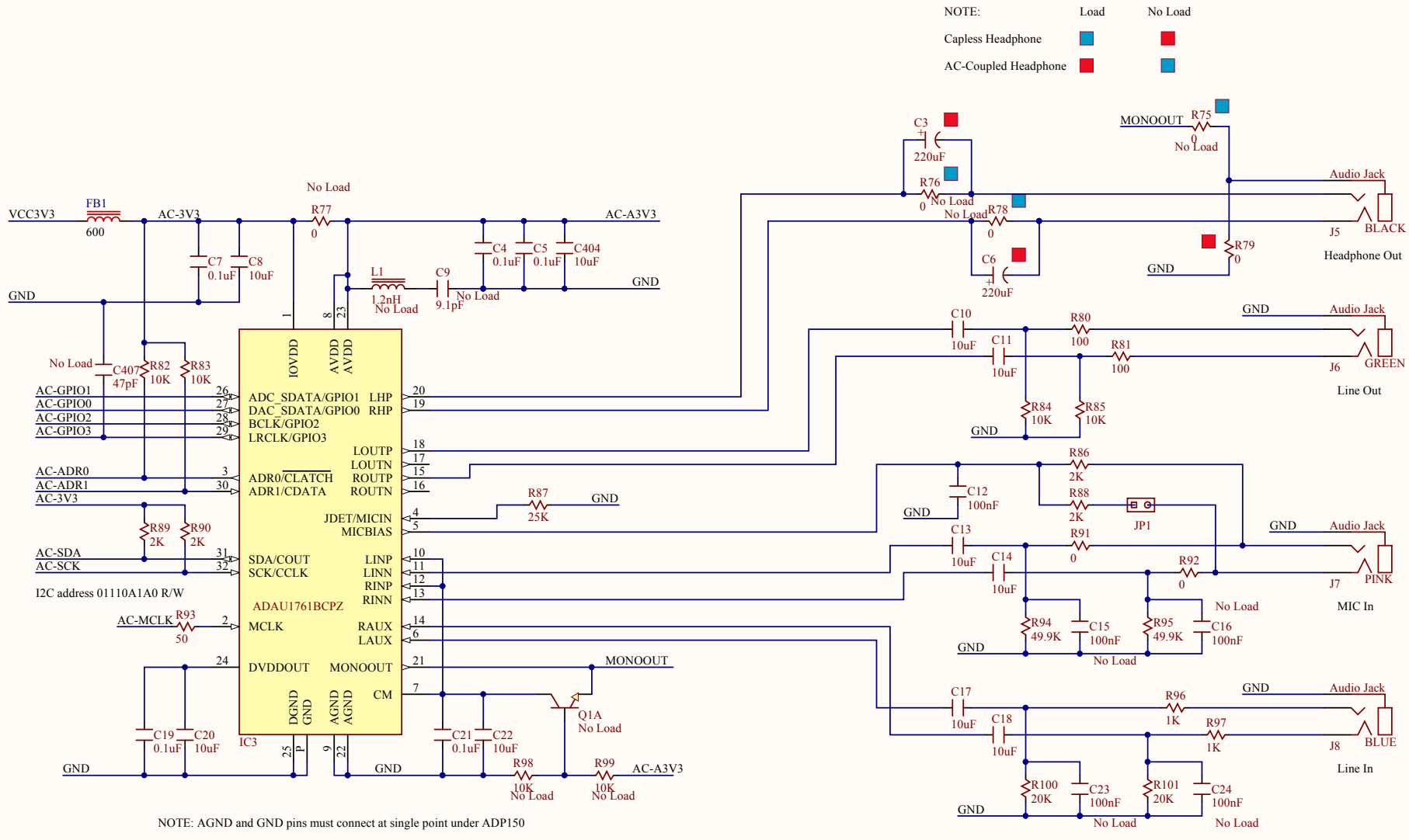
BEYOND THEORY




| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | Audio Codec |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 4 out of 17 |

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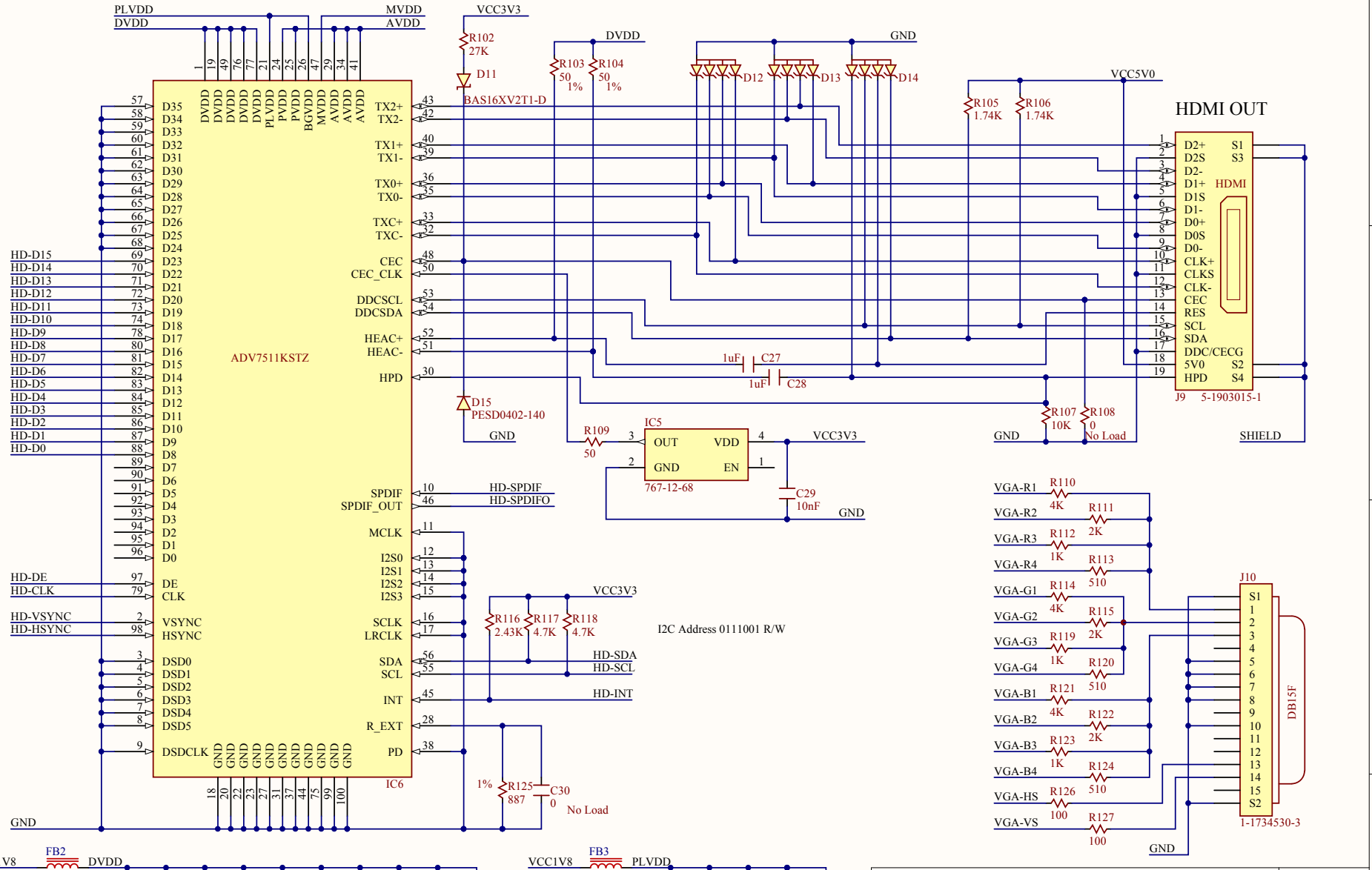
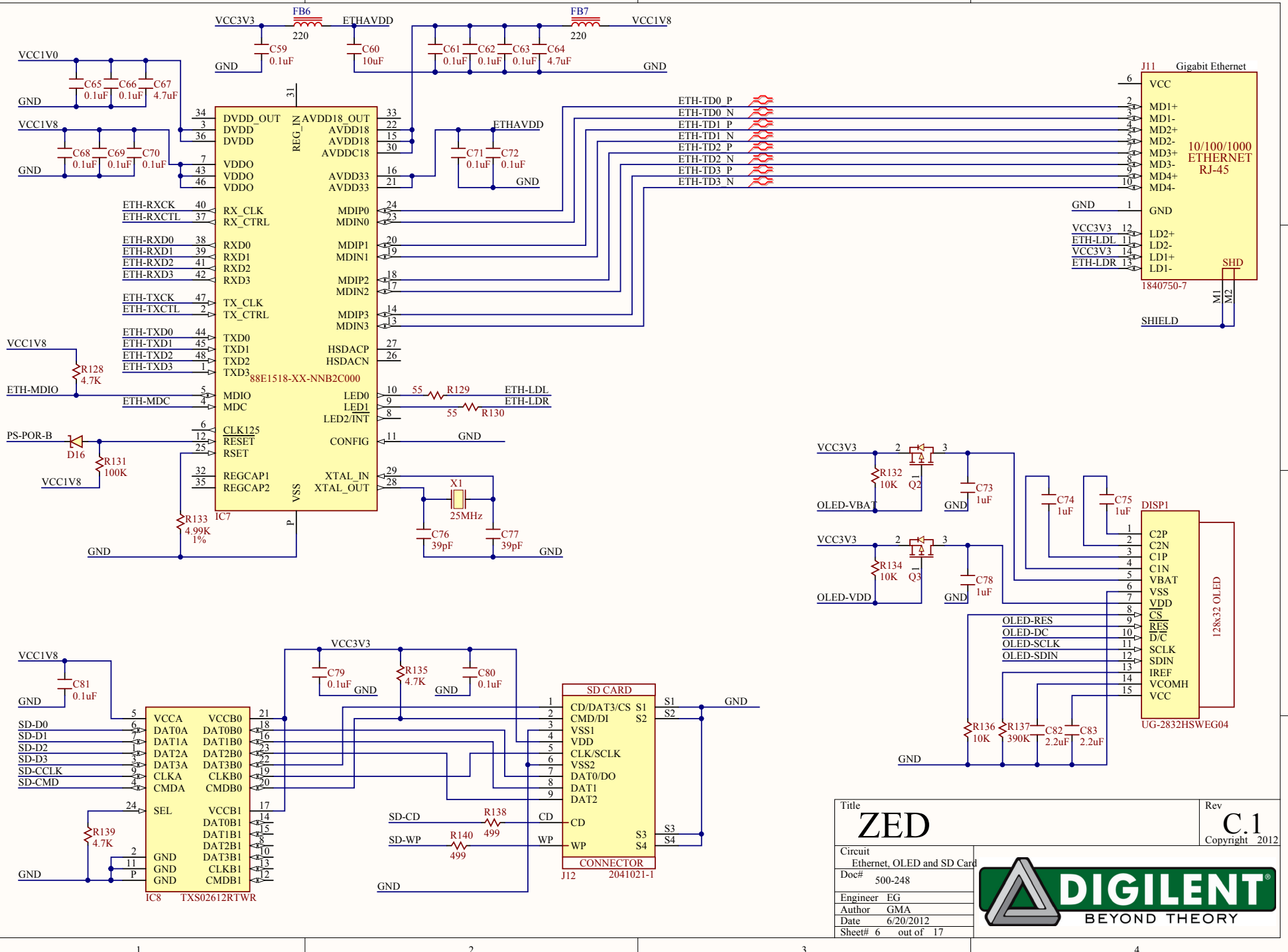
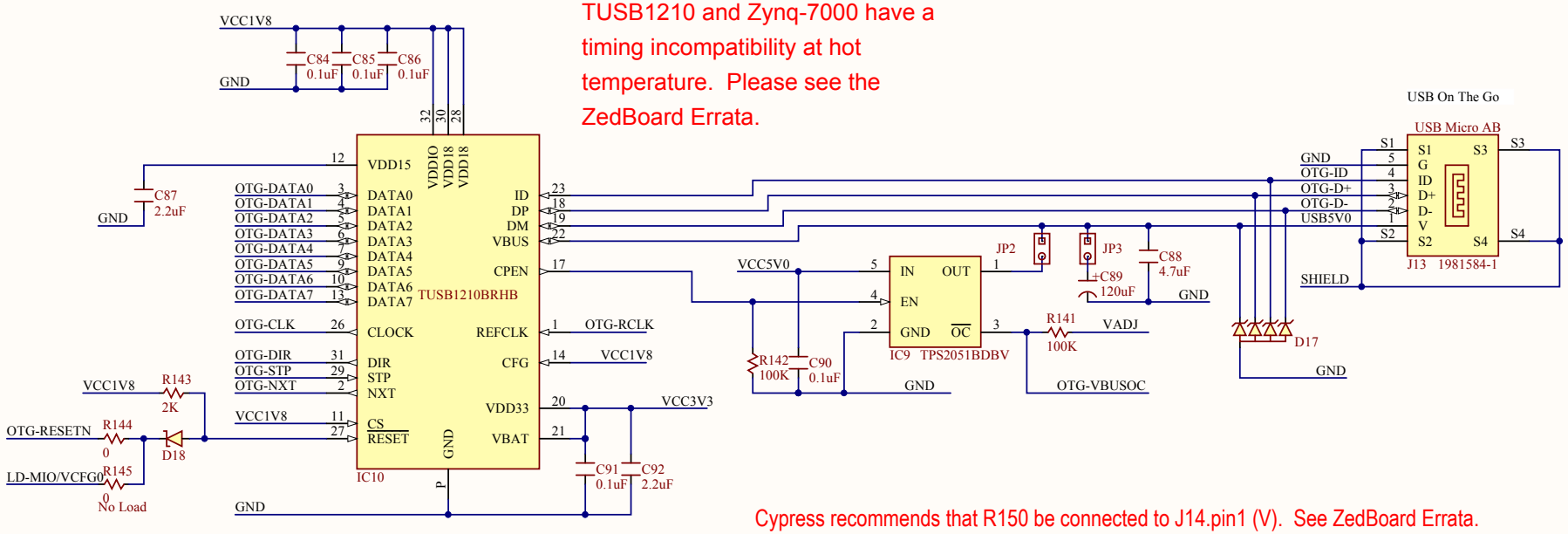
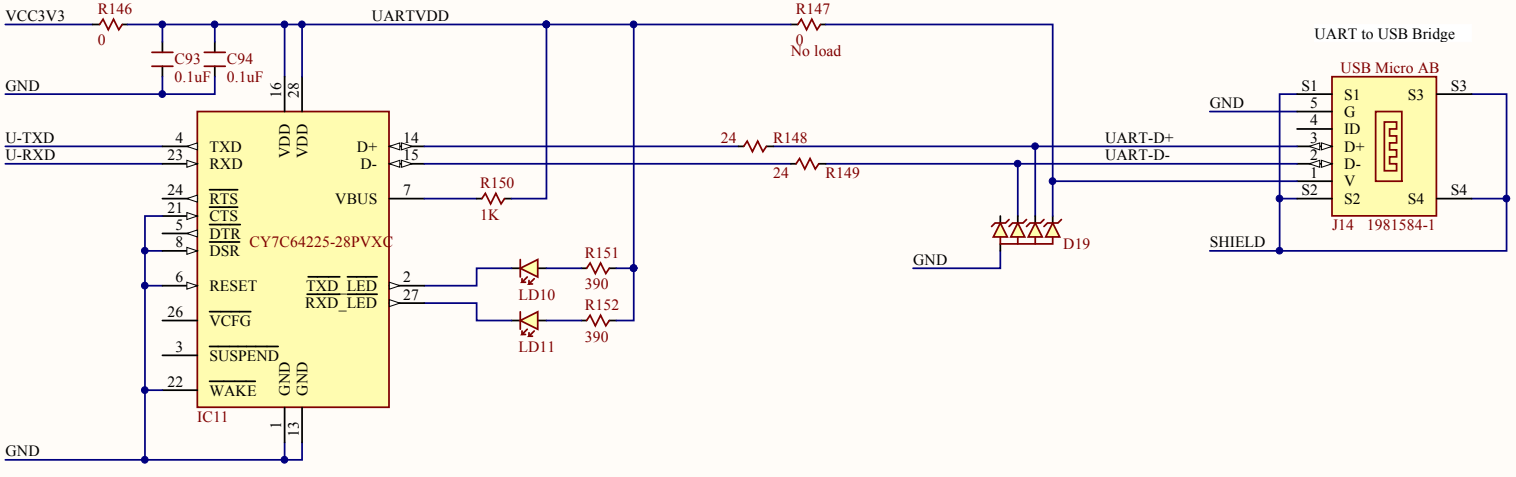

PLVDD
DVDD
MVDD
AVDD
VCC3V3
R102
27K
D11
BAS16XV2T1-D
DVDD
R103
50
1%
R104
50
1%
GND
D12
D13
D14
VCC5V0
R105
1.74K
R106
1.74K
HDMI OUT
ADV7511KSTZ
HD-D15
HD-D14
HD-D13
HD-D12
HD-D11
HD-D10
HD-D9
HD-D8
HD-D7
HD-D6
HD-D5
HD-D4
HD-D3
HD-D2
HD-D1
HD-D0
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
CEC
CEC_CLK
DDCSCL
DDCSDA
HEAC+
HEAC-
HPD
1uF
C27
1uF
C28
D15
PESD0402-140
GND
R109
50
IC5
OUT
VDD
GND
EN
767-12-68
VCC3V3
C29
10nF
GND
R107
10K
R108
0
No Load
GND
SHIELD
J9
5-1903015-1
HDMI
D2+
D2S
D2-
D1+
D1S
D1-
D0+
D0S
D0-
CLK+
CLKS
CLK-
CEC
RES
SCL
SDA
DDC/CECG
5V0
HPD
S1
S3
S2
S4
SPDIF
SPDIF_OUT
HD-SPDIF
HD-SPDIFO
MCLK
I2S0
I2S1
I2S2
I2S3
SCLK
LRCLK
SDA
SCL
INT
R_EXT
PD
HD-DE
HD-CLK
HD-VSYNC
HD-HSYNC
DSD0
DSD1
DSD2
DSD3
DSD4
DSD5
DSDCLK
VSYNC
HSYNC
DE
CLK
R116
2.43K
R117
4.7K
R118
4.7K
VCC3V3
HD-SDA
HD-SCL
HD-INT
I2C Address 0111001 R/W
1%
R125
887
C30
0
No Load
IC6
GND
VGA-R1
VGA-R2
VGA-R3
VGA-R4
VGA-G1
VGA-G2
VGA-G3
VGA-G4
VGA-B1
VGA-B2
VGA-B3
VGA-B4
VGA-HS
VGA-VS
R110
4K
R111
2K
R112
1K
R113
510
R114
4K
R115
2K
R119
1K
R120
510
R121
4K
R122
2K
R123
1K
R124
510
R126
100
R127
100
GND
J10
DB15F
1-1734530-3
VCC1V8
FB2
600
DVDD
C31
10nF
C32
10nF
C33
10nF
C34
10nF
C35
10nF
C36
0.1uF
C37
0.1uF
C38
0.1uF
C39
1uF
C40
10uF
GND
FB4
AVDD
C46
10nF
C47
10nF
C48
10nF
C49
10nF
C50
10nF
C51
0.1uF
C52
0.1uF
C53
0.1uF
C54
1uF
C55
10uF
FB3
PLVDD
C41
10nF
C42
10nF
C43
0.1uF
C44
1uF
C45
10uF
FB5
MVDD
C56
10nF
C57
0.1uF
C58
10uF
Title
ZED
Rev
C.1
Copyright 2012
Circuit
HDMI and VGA
Doc#
500-248
Engineer EG
Author GMA
Date 6/20/2012
Sheet# 5 out of 17
DIGILENT
BEYOND THEORY

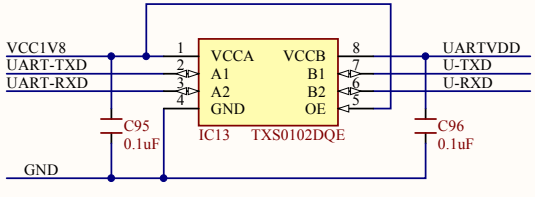

VCC3V3
FB6
220
ETHAVDD
C59 0.1uF
C60 10uF
GND
FB7
220
VCC1V8
C61 0.1uF
C62 0.1uF
C63 0.1uF
C64 4.7uF
VCC1V0
C65 0.1uF
C66 0.1uF
C67 4.7uF
VCC1V8
C68 0.1uF
C69 0.1uF
C70 0.1uF
C71 0.1uF
C72 0.1uF
DVDD_OUT
DVDD
DVDD
VDDO
VDDO
VDDO
REG_IN
AVDD18_OUT
AVDD18
AVDD18
AVDDC18
AVDD33
AVDD33
RX_CLK
RX_CTRL
RXD0
RXD1
RXD2
RXD3
TX_CLK
TX_CTRL
TXD0
TXD1
TXD2
TXD3
MDIO
MDC
CLK125
RESET
RSET
REGCAP1
REGCAP2
VSS
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
HSDACP
HSDACN
LED0
LED1
LED2/INT
CONFIG
XTAL_IN
XTAL_OUT
88E1518-XX-NNB2C000
IC7
ETH-RXCK
ETH-RXCTL
ETH-RXD0
ETH-RXD1
ETH-RXD2
ETH-RXD3
ETH-TXCK
ETH-TXCTL
ETH-TXD0
ETH-TXD1
ETH-TXD2
ETH-TXD3
ETH-MDIO
ETH-MDC
ETH-TD0_P
ETH-TD0_N
ETH-TD1_P
ETH-TD1_N
ETH-TD2_P
ETH-TD2_N
ETH-TD3_P
ETH-TD3_N
R128 4.7K
R129 55
R130 55
ETH-LDL
ETH-LDR
PS-POR-B
D16
R131 100K
R133 4.99K 1%
X1
25MHz
C76 39pF
C77 39pF
J11 Gigabit Ethernet
VCC
MD1+
MD1-
MD2+
MD2-
MD3+
MD3-
MD4+
MD4-
GND
LD2+
LD2-
LD1+
LD1-
SHD
M1
M2
SHIELD
10/100/1000 ETHERNET RJ-45
1840750-7
VCC3V3
ETH-LDL
ETH-LDR
R132 10K
R134 10K
Q2
Q3
C73 1uF
C78 1uF
OLED-VBAT
OLED-VDD
C74 1uF
C75 1uF
DISP1
C2P
C2N
C1P
C1N
VBAT
VSS
VDD
CS
RES
D/C
SCLK
SDIN
IREF
VCOMH
VCC
OLED-RES
OLED-DC
OLED-SCLK
OLED-SDIN
R136 10K
R137 390K
C82 2.2uF
C83 2.2uF
128x32 OLED
UG-2832HSWEG04
C79 0.1uF
R135 4.7K
C80 0.1uF
C81 0.1uF
SD-D0
SD-D1
SD-D2
SD-D3
SD-CCLK
SD-CMD
VCCA
DAT0A
DAT1A
DAT2A
DAT3A
CLKA
CMDA
SEL
GND
GND
P
VCCB0
DAT0B0
DAT1B0
DAT2B0
DAT3B0
CLKB0
CMDB0
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
IC8
TXS02612RTWR
R139 4.7K
SD CARD
CD/DAT3/CS
CMD/DI
VSS1
VDD
CLK/SCLK
VSS2
DAT0/DO
DAT1
DAT2
CD
WP
S1
S2
S3
S4
CONNECTOR
J12
2041021-1
SD-CD
SD-WP
R138 499
R140 499
Title
ZED
Rev
C.1
Copyright 2012
Circuit
Ethernet, OLED and SD Card
Doc# 500-248
Engineer EG
Author GMA
Date 6/20/2012
Sheet# 6 out of 17
DIGILENT
BEYOND THEORY

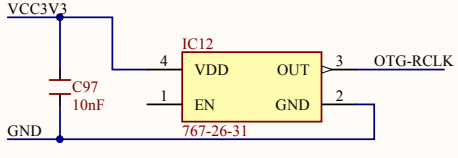
TUSB1210 and Zynq-7000 have a timing incompatibility at hot temperature. Please see the ZedBoard Errata.




Cypress recommends that R150 be connected to J14.pin1 (V). See ZedBoard Errata.




| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | USB and UART |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 7 out of 17 |

DIGILENT BEYOND THEORY

Xilinx JTAG Header

2x7
2mm Header
J15

VCC3V3
TMS-JTAG
TCK-JTAG
TDO-JTAG
TDI-JTAG
PROG-RST
GND

R153 100 TMS
R154 100 TCK
R155 100 TDO-USB/TDI-FPGA
R156 50 TDI-USB

From USB
D20
GND

Heatsink
BDN09-3CB/A01
See ZedBoard Errata
for more info

BANK 0
IC16A XC7Z020CLG484

TMS G12 TMS
TCK G11 TCK
TDI H13 TDO-USB/TDI-FPGA
TDO G14 TDO-FPGA

RSVDVCC T10 VCC3V3
RSVDVCC T8
RSVDVCC T7
RSVDGND G10 GND

DONE T12
PROGRAM_B T11 PROG
INIT_B T14

DXN N12 XADC-DXN
DXP N11 XADC-DXP

VP L11 XADC-VP-R
VN M12 XADC-VN-R

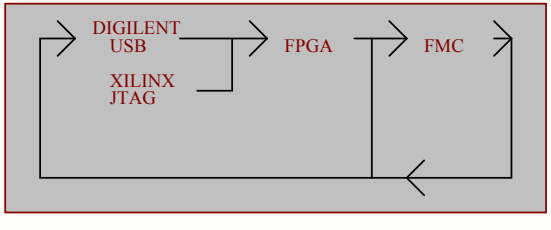
CFGBVS T13
R160 10K VCC3V3
No Load
JP4 GND

VCC3V3
R158 4.7K
R159 270
BLUE LD12
GND

VCC3V3
R161 4.7K
PROG
BTN6 GND

XADC-VP R162 100 XADC-VP-R
XADC-VN R163 100 XADC-VN-R
1nF C99

JTAG SCAN CHAIN




VCC3V3
C98 0.1uF
GND
R157 330

IC14
SPI-DQ0/MODE0 5 SDI/DQ0 VCC 8
SPI-DQ1/MODE1 2 SDO/DQ1 SCK 6 SPI-SCK/MODE4
SPI-DQ2/MODE2 3 WP/DQ2 CS 1 SPI-CS
SPI-DQ3/MODE3 7 HOLD/DQ3 VSS 4 GND
S25FL256SAGNFI00
No Load

Note: Load either package, not both. Default SOIC16

VCC3V3
IC15
SPI-DQ0/MODE0 15 SDI/DQ0 VCC 2
SPI-DQ1/MODE1 8 SDO/DQ1 SCK 16 SPI-SCK/MODE4
SPI-DQ2/MODE2 9 WP/DQ2 CS 7 SPI-CS
SPI-DQ3/MODE3 1 HOLD/DQ3 VSS 10 GND
S25FL256SAGMFI00

| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | FPGA Configuration |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 8 out of 17 |

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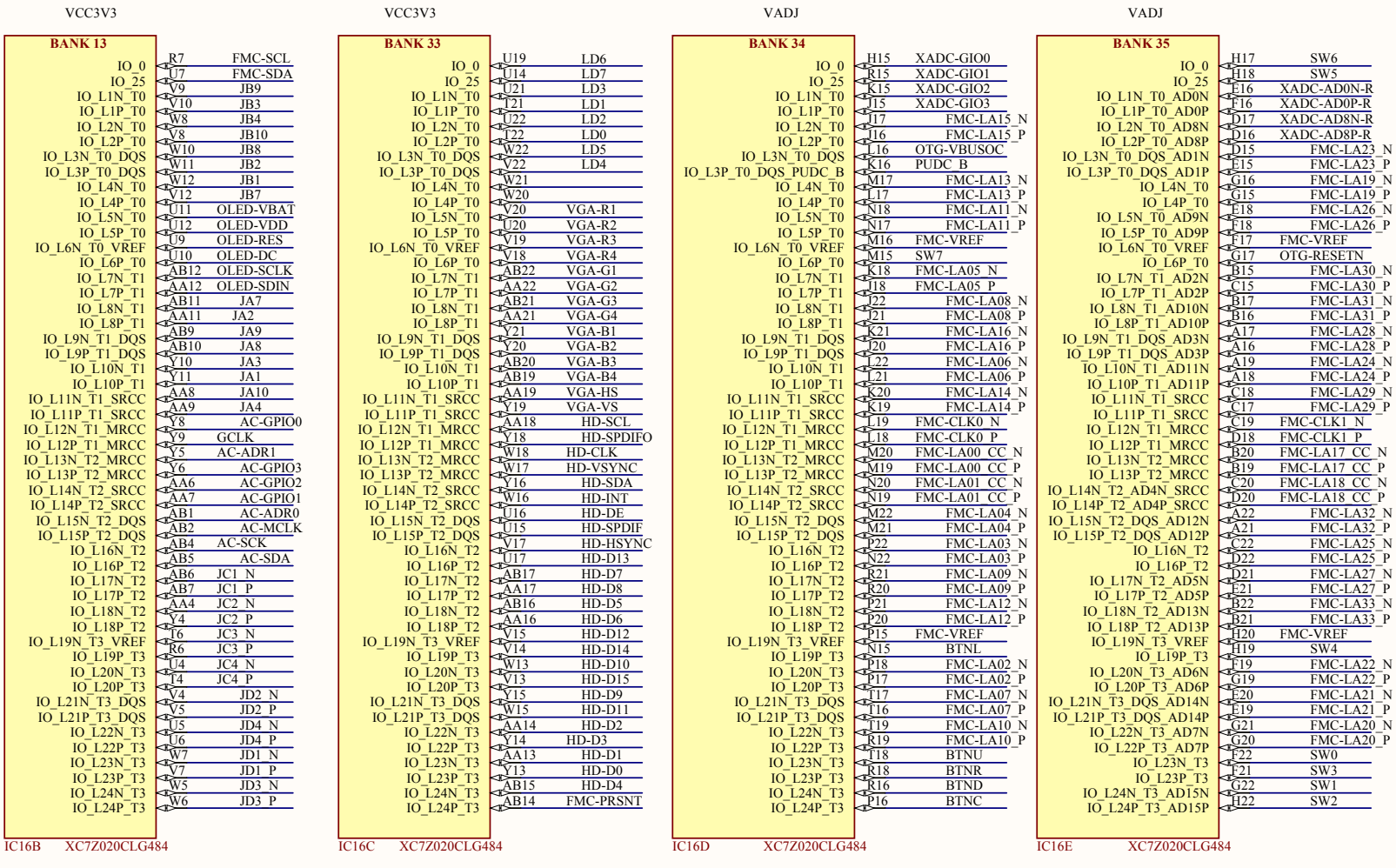
BEYOND THEORY


VCC3V3
BANK 13
IO_0 R7 FMC-SCL
IO_25 U7 FMC-SDA
IO_L1N_T0 V9 JB9
IO_L1P_T0 V10 JB3
IO_L2N_T0 W8 JB4
IO_L2P_T0 V8 JB10
IO_L3N_T0_DQS W10 JB8
IO_L3P_T0_DQS W11 JB2
IO_L4N_T0 W12 JB1
IO_L4P_T0 V12 JB7
IO_L5N_T0 U11 OLED-VBAT
IO_L5P_T0 U12 OLED-VDD
IO_L6N_T0_VREF U9 OLED-RES
IO_L6P_T0 U10 OLED-DC
IO_L7N_T1 AB12 OLED-SCLK
IO_L7P_T1 AA12 OLED-SDIN
IO_L8N_T1 AB11 JA7
IO_L8P_T1 AA11 JA2
IO_L9N_T1_DQS AB9 JA9
IO_L9P_T1_DQS AB10 JA8
IO_L10N_T1 Y10 JA3
IO_L10P_T1 Y11 JA1
IO_L11N_T1_SRCC AA8 JA10
IO_L11P_T1_SRCC AA9 JA4
IO_L12N_T1_MRCC Y8 AC-GPIO0
IO_L12P_T1_MRCC Y9 GCLK
IO_L13N_T2_MRCC Y5 AC-ADR1
IO_L13P_T2_MRCC Y6 AC-GPIO3
IO_L14N_T2_SRCC AA6 AC-GPIO2
IO_L14P_T2_SRCC AA7 AC-GPIO1
IO_L15N_T2_DQS AB1 AC-ADR0
IO_L15P_T2_DQS AB2 AC-MCLK
IO_L16N_T2 AB4 AC-SCK
IO_L16P_T2 AB5 AC-SDA
IO_L17N_T2 AB6 JC1_N
IO_L17P_T2 AB7 JC1_P
IO_L18N_T2 AA4 JC2_N
IO_L18P_T2 Y4 JC2_P
IO_L19N_T3_VREF T6 JC3_N
IO_L19P_T3 R6 JC3_P
IO_L20N_T3 U4 JC4_N
IO_L20P_T3 T4 JC4_P
IO_L21N_T3_DQS V4 JD2_N
IO_L21P_T3_DQS V5 JD2_P
IO_L22N_T3 U5 JD4_N
IO_L22P_T3 U6 JD4_P
IO_L23N_T3 W7 JD1_N
IO_L23P_T3 V7 JD1_P
IO_L24N_T3 W5 JD3_N
IO_L24P_T3 W6 JD3_P
IC16B XC7Z020CLG484
VCC3V3
BANK 33
IO_0 U19 LD6
IO_25 U14 LD7
IO_L1N_T0 U21 LD3
IO_L1P_T0 T21 LD1
IO_L2N_T0 U22 LD2
IO_L2P_T0 T22 LD0
IO_L3N_T0_DQS W22 LD5
IO_L3P_T0_DQS V22 LD4
IO_L4N_T0 W21
IO_L4P_T0 W20
IO_L5N_T0 V20 VGA-R1
IO_L5P_T0 U20 VGA-R2
IO_L6N_T0_VREF V19 VGA-R3
IO_L6P_T0 V18 VGA-R4
IO_L7N_T1 AB22 VGA-G1
IO_L7P_T1 AA22 VGA-G2
IO_L8N_T1 AB21 VGA-G3
IO_L8P_T1 AA21 VGA-G4
IO_L9N_T1_DQS Y21 VGA-B1
IO_L9P_T1_DQS Y20 VGA-B2
IO_L10N_T1 AB20 VGA-B3
IO_L10P_T1 AB19 VGA-B4
IO_L11N_T1_SRCC AA19 VGA-HS
IO_L11P_T1_SRCC Y19 VGA-VS
IO_L12N_T1_MRCC AA18 HD-SCL
IO_L12P_T1_MRCC Y18 HD-SPDIFO
IO_L13N_T2_MRCC W18 HD-CLK
IO_L13P_T2_MRCC W17 HD-VSYNC
IO_L14N_T2_SRCC Y16 HD-SDA
IO_L14P_T2_SRCC W16 HD-INT
IO_L15N_T2_DQS U16 HD-DE
IO_L15P_T2_DQS U15 HD-SPDIF
IO_L16N_T2 V17 HD-HSYNC
IO_L16P_T2 U17 HD-D13
IO_L17N_T2 AB17 HD-D7
IO_L17P_T2 AA17 HD-D8
IO_L18N_T2 AB16 HD-D5
IO_L18P_T2 AA16 HD-D6
IO_L19N_T3_VREF V15 HD-D12
IO_L19P_T3 V14 HD-D14
IO_L20N_T3 W13 HD-D10
IO_L20P_T3 V13 HD-D15
IO_L21N_T3_DQS Y15 HD-D9
IO_L21P_T3_DQS W15 HD-D11
IO_L22N_T3 AA14 HD-D2
IO_L22P_T3 Y14 HD-D3
IO_L23N_T3 AA13 HD-D1
IO_L23P_T3 Y13 HD-D0
IO_L24N_T3 AB15 HD-D4
IO_L24P_T3 AB14 FMC-PRSNT
IC16C XC7Z020CLG484
VADJ
BANK 34
IO_0 H15 XADC-GIO0
IO_25 R15 XADC-GIO1
IO_L1N_T0 K15 XADC-GIO2
IO_L1P_T0 I15 XADC-GIO3
IO_L2N_T0 J17 FMC-LA15_N
IO_L2P_T0 J16 FMC-LA15_P
IO_L3N_T0_DQS L16 OTG-VBUSOC
IO_L3P_T0_DQS_PUDC_B K16 PUDC_B
IO_L4N_T0 M17 FMC-LA13_N
IO_L4P_T0 L17 FMC-LA13_P
IO_L5N_T0 N18 FMC-LA11_N
IO_L5P_T0 N17 FMC-LA11_P
IO_L6N_T0_VREF M16 FMC-VREF
IO_L6P_T0 M15 SW7
IO_L7N_T1 K18 FMC-LA05_N
IO_L7P_T1 I18 FMC-LA05_P
IO_L8N_T1 J22 FMC-LA08_N
IO_L8P_T1 J21 FMC-LA08_P
IO_L9N_T1_DQS K21 FMC-LA16_N
IO_L9P_T1_DQS J20 FMC-LA16_P
IO_L10N_T1 L22 FMC-LA06_N
IO_L10P_T1 L21 FMC-LA06_P
IO_L11N_T1_SRCC K20 FMC-LA14_N
IO_L11P_T1_SRCC K19 FMC-LA14_P
IO_L12N_T1_MRCC L19 FMC-CLK0_N
IO_L12P_T1_MRCC L18 FMC-CLK0_P
IO_L13N_T2_MRCC M20 FMC-LA00_CC_N
IO_L13P_T2_MRCC M19 FMC-LA00_CC_P
IO_L14N_T2_SRCC N20 FMC-LA01_CC_N
IO_L14P_T2_SRCC N19 FMC-LA01_CC_P
IO_L15N_T2_DQS M22 FMC-LA04_N
IO_L15P_T2_DQS M21 FMC-LA04_P
IO_L16N_T2 P22 FMC-LA03_N
IO_L16P_T2 N22 FMC-LA03_P
IO_L17N_T2 R21 FMC-LA09_N
IO_L17P_T2 R20 FMC-LA09_P
IO_L18N_T2 P21 FMC-LA12_N
IO_L18P_T2 P20 FMC-LA12_P
IO_L19N_T3_VREF P15 FMC-VREF
IO_L19P_T3 N15 BTNL
IO_L20N_T3 P18 FMC-LA02_N
IO_L20P_T3 P17 FMC-LA02_P
IO_L21N_T3_DQS T17 FMC-LA07_N
IO_L21P_T3_DQS T16 FMC-LA07_P
IO_L22N_T3 T19 FMC-LA10_N
IO_L22P_T3 R19 FMC-LA10_P
IO_L23N_T3 T18 BTNU
IO_L23P_T3 R18 BTNR
IO_L24N_T3 R16 BTND
IO_L24P_T3 P16 BTNC
IC16D XC7Z020CLG484
VADJ
BANK 35
IO_0 H17 SW6
IO_25 H18 SW5
IO_L1N_T0_AD0N E16 XADC-AD0N-R
IO_L1P_T0_AD0P F16 XADC-AD0P-R
IO_L2N_T0_AD8N D17 XADC-AD8N-R
IO_L2P_T0_AD8P D16 XADC-AD8P-R
IO_L3N_T0_DQS_AD1N D15 FMC-LA23_N
IO_L3P_T0_DQS_AD1P E15 FMC-LA23_P
IO_L4N_T0 G16 FMC-LA19_N
IO_L4P_T0 G15 FMC-LA19_P
IO_L5N_T0_AD9N E18 FMC-LA26_N
IO_L5P_T0_AD9P E18 FMC-LA26_P
IO_L6N_T0_VREF F17 FMC-VREF
IO_L6P_T0 G17 OTG-RESETN
IO_L7N_T1_AD2N B15 FMC-LA30_N
IO_L7P_T1_AD2P C15 FMC-LA30_P
IO_L8N_T1_AD10N B17 FMC-LA31_N
IO_L8P_T1_AD10P B16 FMC-LA31_P
IO_L9N_T1_DQS_AD3N A17 FMC-LA28_N
IO_L9P_T1_DQS_AD3P A16 FMC-LA28_P
IO_L10N_T1_AD11N A19 FMC-LA24_N
IO_L10P_T1_AD11P A18 FMC-LA24_P
IO_L11N_T1_SRCC C18 FMC-LA29_N
IO_L11P_T1_SRCC C17 FMC-LA29_P
IO_L12N_T1_MRCC C19 FMC-CLK1_N
IO_L12P_T1_MRCC D18 FMC-CLK1_P
IO_L13N_T2_MRCC B20 FMC-LA17_CC_N
IO_L13P_T2_MRCC B19 FMC-LA17_CC_P
IO_L14N_T2_AD4N_SRCC C20 FMC-LA18_CC_N
IO_L14P_T2_AD4P_SRCC D20 FMC-LA18_CC_P
IO_L15N_T2_DQS_AD12N A22 FMC-LA32_N
IO_L15P_T2_DQS_AD12P A21 FMC-LA32_P
IO_L16N_T2 C22 FMC-LA25_N
IO_L16P_T2 D22 FMC-LA25_P
IO_L17N_T2_AD5N D21 FMC-LA27_N
IO_L17P_T2_AD5P E21 FMC-LA27_P
IO_L18N_T2_AD13N B22 FMC-LA33_N
IO_L18P_T2_AD13P B21 FMC-LA33_P
IO_L19N_T3_VREF H20 FMC-VREF
IO_L19P_T3 H19 SW4
IO_L20N_T3_AD6N F19 FMC-LA22_N
IO_L20P_T3_AD6P G19 FMC-LA22_P
IO_L21N_T3_DQS_AD14N E20 FMC-LA21_N
IO_L21P_T3_DQS_AD14P E19 FMC-LA21_P
IO_L22N_T3_AD7N G21 FMC-LA20_N
IO_L22P_T3_AD7P G20 FMC-LA20_P
IO_L23N_T3 F22 SW0
IO_L23P_T3 F21 SW3
IO_L24N_T3_AD15N G22 SW1
IO_L24P_T3_AD15P H22 SW2
IC16E XC7Z020CLG484
PUDC_B
R164
1K
R165
10K
VADJ
GND
No Load
JP5
VCC3V3
IC17
VDD
OUT
EN
GND
767-100-136
GCLK
C101
10nF
GND
XADC-AD0_N
R166
100
XADC-AD0N-R
1nF
C100
XADC-AD0_P
R167
100
XADC-AD0P-R
XADC-AD8_N
R168
100
XADC-AD8N-R
1nF
C102
XADC-AD8_P
R169
100
XADC-AD8P-R
Title
ZED
Rev
C.1
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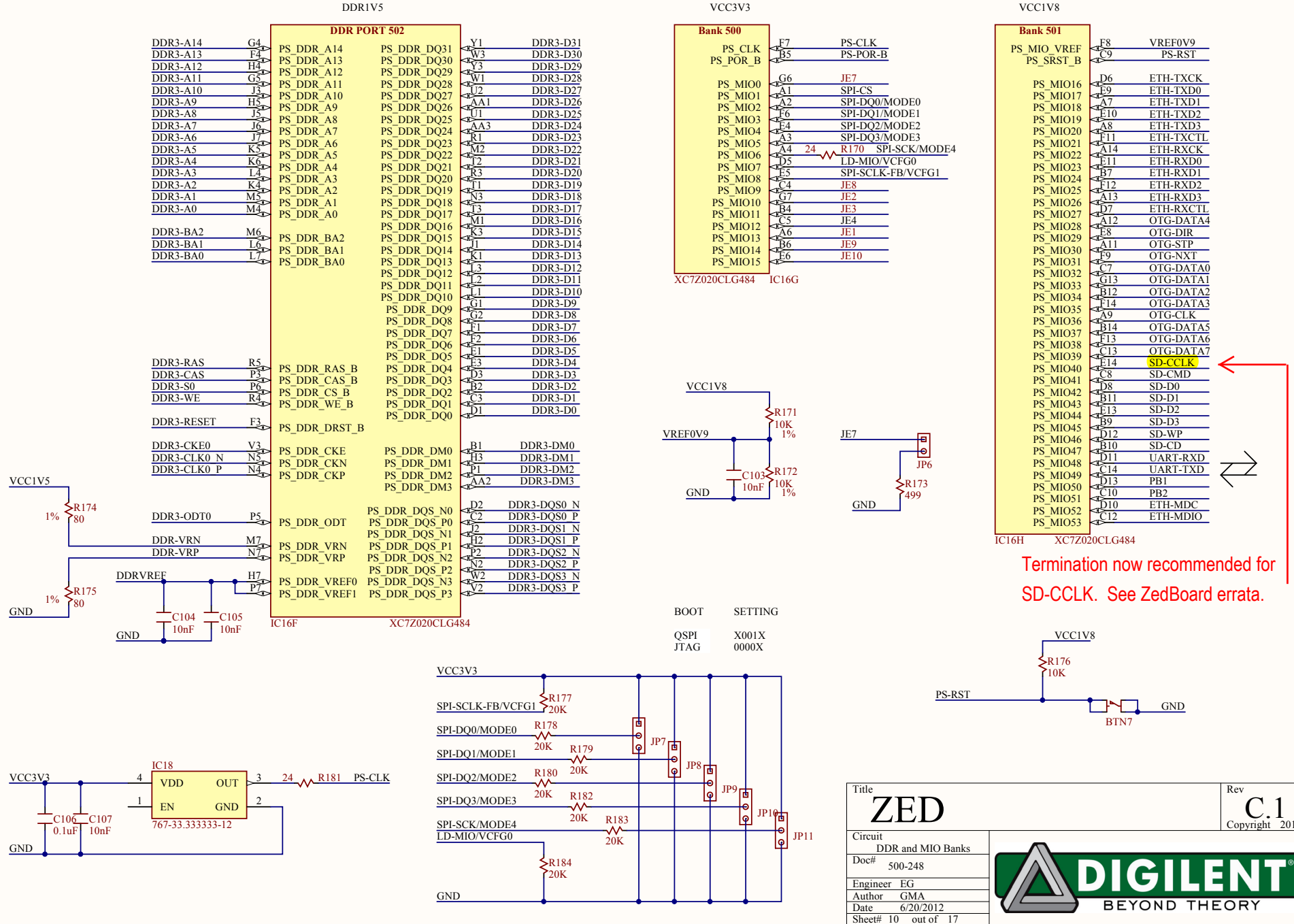
Circuit
FPGA Banks
Doc#
500-248
Engineer EG
Author GMA
Date 6/20/2012
Sheet# 9 out of 17
DIGILENT
BEYOND THEORY


DDR1V5
DDR PORT 502
DDR3-A14 G4
DDR3-A13 F4
DDR3-A12 H4
DDR3-A11 G5
DDR3-A10 J3
DDR3-A9 H5
DDR3-A8 J5
DDR3-A7 J6
DDR3-A6 J7
DDR3-A5 K5
DDR3-A4 K6
DDR3-A3 L4
DDR3-A2 K4
DDR3-A1 M5
DDR3-A0 M4
DDR3-BA2 M6
DDR3-BA1 L6
DDR3-BA0 L7
DDR3-RAS R5
DDR3-CAS P3
DDR3-S0 P6
DDR3-WE R4
DDR3-RESET F3
DDR3-CKE0 V3
DDR3-CLK0_N N5
DDR3-CLK0_P N4
DDR3-ODT0 P5
DDR-VRN M7
DDR-VRP N7
DDRVREF H7
P7
PS_DDR_A14
PS_DDR_A13
PS_DDR_A12
PS_DDR_A11
PS_DDR_A10
PS_DDR_A9
PS_DDR_A8
PS_DDR_A7
PS_DDR_A6
PS_DDR_A5
PS_DDR_A4
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A0
PS_DDR_BA2
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_RAS_B
PS_DDR_CAS_B
PS_DDR_CS_B
PS_DDR_WE_B
PS_DDR_DRST_B
PS_DDR_CKE
PS_DDR_CKN
PS_DDR_CKP
PS_DDR_ODT
PS_DDR_VRN
PS_DDR_VRP
PS_DDR_VREF0
PS_DDR_VREF1
PS_DDR_DQ31 Y1 DDR3-D31
PS_DDR_DQ30 W3 DDR3-D30
PS_DDR_DQ29 Y3 DDR3-D29
PS_DDR_DQ28 W1 DDR3-D28
PS_DDR_DQ27 U2 DDR3-D27
PS_DDR_DQ26 AA1 DDR3-D26
PS_DDR_DQ25 U1 DDR3-D25
PS_DDR_DQ24 AA3 DDR3-D24
PS_DDR_DQ23 R1 DDR3-D23
PS_DDR_DQ22 M2 DDR3-D22
PS_DDR_DQ21 P2 DDR3-D21
PS_DDR_DQ20 R3 DDR3-D20
PS_DDR_DQ19 T1 DDR3-D19
PS_DDR_DQ18 N3 DDR3-D18
PS_DDR_DQ17 T3 DDR3-D17
PS_DDR_DQ16 M1 DDR3-D16
PS_DDR_DQ15 K3 DDR3-D15
PS_DDR_DQ14 J1 DDR3-D14
PS_DDR_DQ13 K1 DDR3-D13
PS_DDR_DQ12 L3 DDR3-D12
PS_DDR_DQ11 L2 DDR3-D11
PS_DDR_DQ10 L1 DDR3-D10
PS_DDR_DQ9 G1 DDR3-D9
PS_DDR_DQ8 G2 DDR3-D8
PS_DDR_DQ7 F1 DDR3-D7
PS_DDR_DQ6 F2 DDR3-D6
PS_DDR_DQ5 E1 DDR3-D5
PS_DDR_DQ4 E3 DDR3-D4
PS_DDR_DQ3 D3 DDR3-D3
PS_DDR_DQ2 B2 DDR3-D2
PS_DDR_DQ1 C3 DDR3-D1
PS_DDR_DQ0 D1 DDR3-D0
PS_DDR_DM0 B1 DDR3-DM0
PS_DDR_DM1 H3 DDR3-DM1
PS_DDR_DM2 P1 DDR3-DM2
PS_DDR_DM3 AA2 DDR3-DM3
PS_DDR_DQS_N0 D2 DDR3-DQS0_N
PS_DDR_DQS_P0 C2 DDR3-DQS0_P
PS_DDR_DQS_N1 J2 DDR3-DQS1_N
PS_DDR_DQS_P1 H2 DDR3-DQS1_P
PS_DDR_DQS_N2 P2 DDR3-DQS2_N
PS_DDR_DQS_P2 N2 DDR3-DQS2_P
PS_DDR_DQS_N3 W2 DDR3-DQS3_N
PS_DDR_DQS_P3 V2 DDR3-DQS3_P
IC16F
XC7Z020CLG484
VCC1V5
R174 1% 80
R175 1% 80
GND
C104 10nF
C105 10nF
VCC3V3
Bank 500
PS_CLK F7 PS-CLK
PS_POR_B B5 PS-POR-B
PS_MIO0 G6 JE7
PS_MIO1 A1 SPI-CS
PS_MIO2 A2 SPI-DQ0/MODE0
PS_MIO3 F6 SPI-DQ1/MODE1
PS_MIO4 E4 SPI-DQ2/MODE2
PS_MIO5 A3 SPI-DQ3/MODE3
PS_MIO6 A4 24 R170 SPI-SCK/MODE4
PS_MIO7 D5 LD-MIO/VCFG0
PS_MIO8 E5 SPI-SCLK-FB/VCFG1
PS_MIO9 C4 JE8
PS_MIO10 G7 JE2
PS_MIO11 B4 JE3
PS_MIO12 C5 JE4
PS_MIO13 A6 JE1
PS_MIO14 B6 JE9
PS_MIO15 E6 JE10
XC7Z020CLG484 IC16G
VCC1V8
R171 10K 1%
VREF0V9
C103 10nF
R172 10K 1%
GND
JE7
JP6
R173 499
GND
VCC1V8
Bank 501
PS_MIO_VREF F8 VREF0V9
PS_SRST_B C9 PS-RST
PS_MIO16 D6 ETH-TXCK
PS_MIO17 E9 ETH-TXD0
PS_MIO18 A7 ETH-TXD1
PS_MIO19 E10 ETH-TXD2
PS_MIO20 A8 ETH-TXD3
PS_MIO21 F11 ETH-TXCTL
PS_MIO22 A14 ETH-RXCK
PS_MIO23 E11 ETH-RXD0
PS_MIO24 B7 ETH-RXD1
PS_MIO25 F12 ETH-RXD2
PS_MIO26 A13 ETH-RXD3
PS_MIO27 D7 ETH-RXCTL
PS_MIO28 A12 OTG-DATA4
PS_MIO29 E8 OTG-DIR
PS_MIO30 A11 OTG-STP
PS_MIO31 F9 OTG-NXT
PS_MIO32 C7 OTG-DATA0
PS_MIO33 G13 OTG-DATA1
PS_MIO34 B12 OTG-DATA2
PS_MIO35 F14 OTG-DATA3
PS_MIO36 A9 OTG-CLK
PS_MIO37 B14 OTG-DATA5
PS_MIO38 F13 OTG-DATA6
PS_MIO39 C13 OTG-DATA7
PS_MIO40 E14 SD-CCLK
PS_MIO41 C8 SD-CMD
PS_MIO42 D8 SD-D0
PS_MIO43 B11 SD-D1
PS_MIO44 E13 SD-D2
PS_MIO45 B9 SD-D3
PS_MIO46 D12 SD-WP
PS_MIO47 B10 SD-CD
PS_MIO48 D11 UART-RXD
PS_MIO49 C14 UART-TXD
PS_MIO50 D13 PB1
PS_MIO51 C10 PB2
PS_MIO52 D10 ETH-MDC
PS_MIO53 C12 ETH-MDIO
IC16H
XC7Z020CLG484
Termination now recommended for SD-CCLK. See ZedBoard errata.
BOOT SETTING
QSPI X001X
JTAG 0000X
VCC1V8
R176 10K
PS-RST
GND
BTN7
VCC3V3
IC18
VDD OUT
EN GND
767-33.333333-12
24 R181 PS-CLK
C106 0.1uF
C107 10nF
GND
VCC3V3
SPI-SCLK-FB/VCFG1 R177 20K
SPI-DQ0/MODE0 R178 20K
SPI-DQ1/MODE1 R179 20K
SPI-DQ2/MODE2 R180 20K
SPI-DQ3/MODE3 R182 20K
SPI-SCK/MODE4 R183 20K
LD-MIO/VCFG0
R184 20K
GND
JP7
JP8
JP9
JP10
JP11
Title
ZED
Rev
C.1
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Circuit
DDR and MIO Banks
Doc# 500-248
Engineer EG
Author GMA
Date 6/20/2012
Sheet# 10 out of 17
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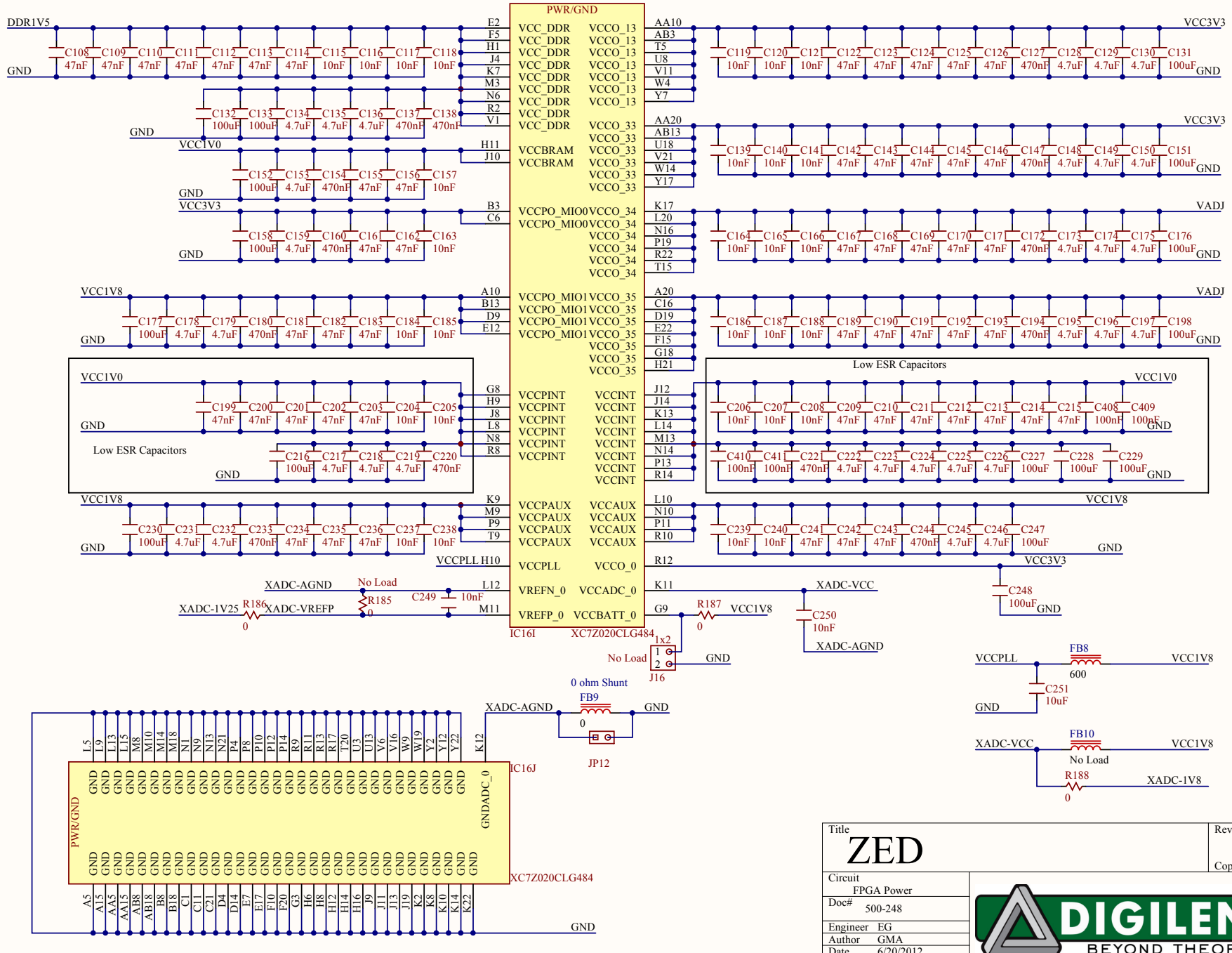


| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Circuit | FPGA Power |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 11 out of 17 |



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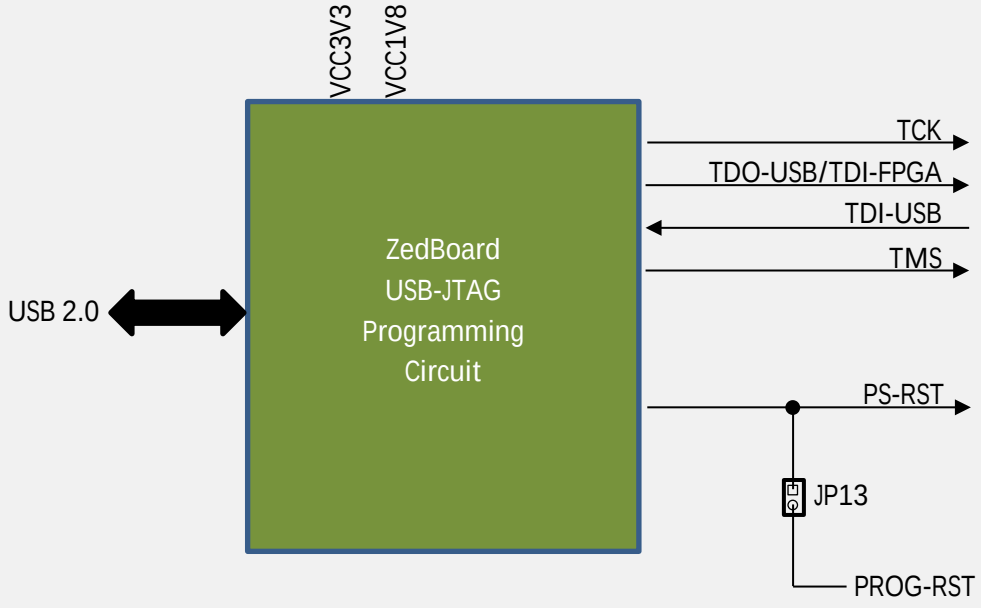


The ZedBoard contains a proprietary USB-JTAG circuit which is obscured on this sheet. This circuit contains IC19, IC20, IC21, IC22, IC23, IC24, JP13, and J17, along with a number of resistors and capacitors. The firmware for this circuit is not publicly available. However, the firmware does come pre-programmed in the SMT2 USB-JTAG module available from Digilent and Avnet. For more information, please see

www.em.avnet.com/jtagsmt2

| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Circuit | USB Programming |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
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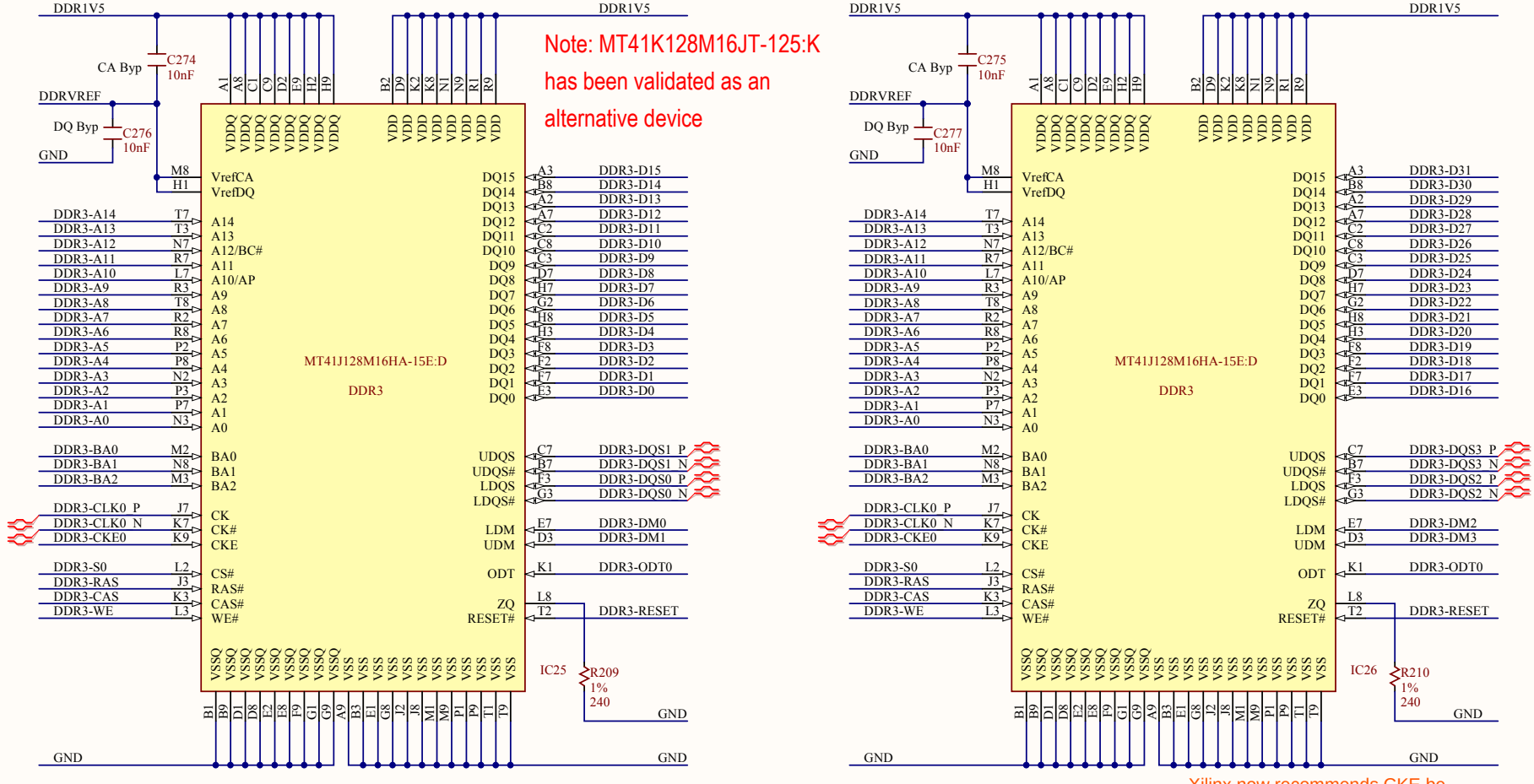
Note: MT41K128M16JT-125:K has been validated as an alternative device
MT41J128M16HA-15E:D
DDR3
IC25
IC26
R209 1% 240
R210 1% 240
The DDR3 symbol used in the Rev C ZedBoard has a mistake that improperly leaves Pins F1 and G7 disconnected. This affects IC25 and IC26. See ZedBoard Errata.
Xilinx now recommends CKE be pulled up through 40ohms to Vtt
R211 4.7K
R212 4.7K
Title ZED
Rev C.1
Copyright 2012
Circuit DDR3 Memory
Doc# 500-248
Engineer EG
Author GMA
Date 6/20/2012
Sheet# 13 out of 17
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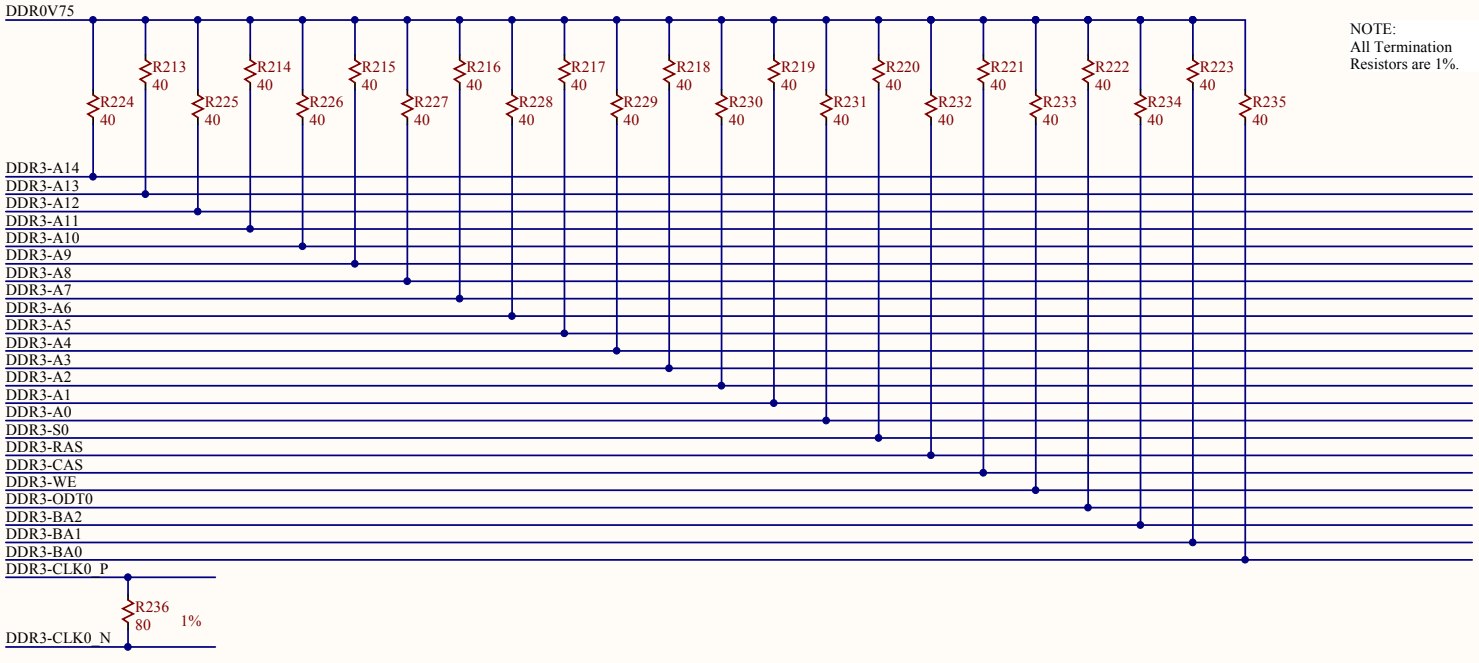
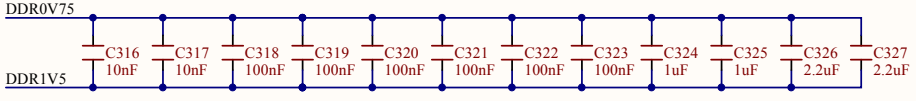
# DDR3 TERMINATION




NOTE:
All Termination Resistors are 1%.




| | |
|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | DDR3 Termination |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
| Sheet# | 14 out of 17 |

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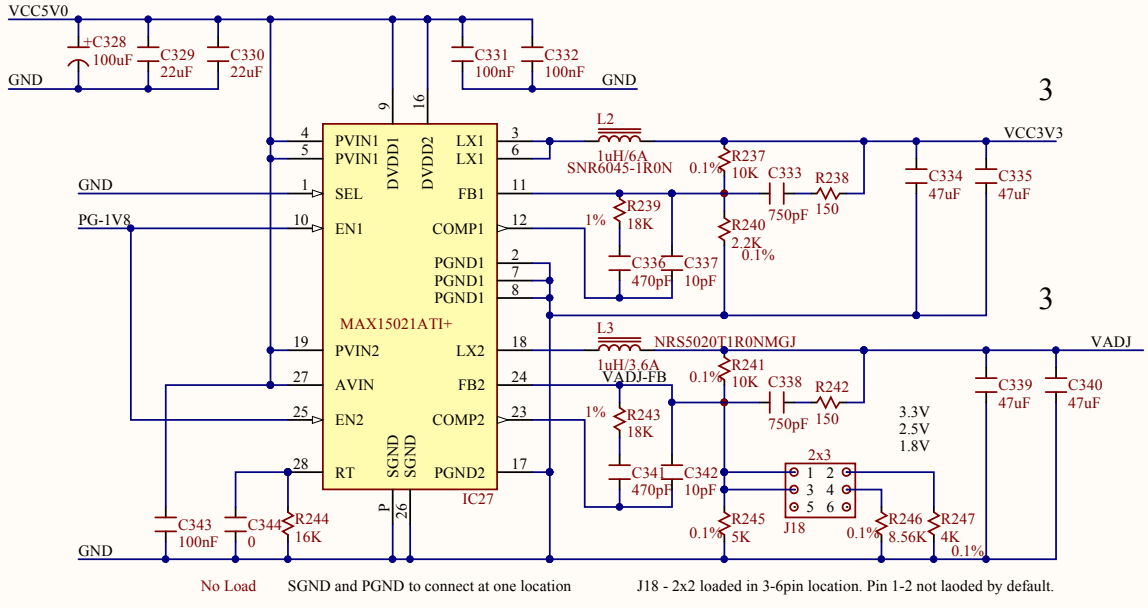
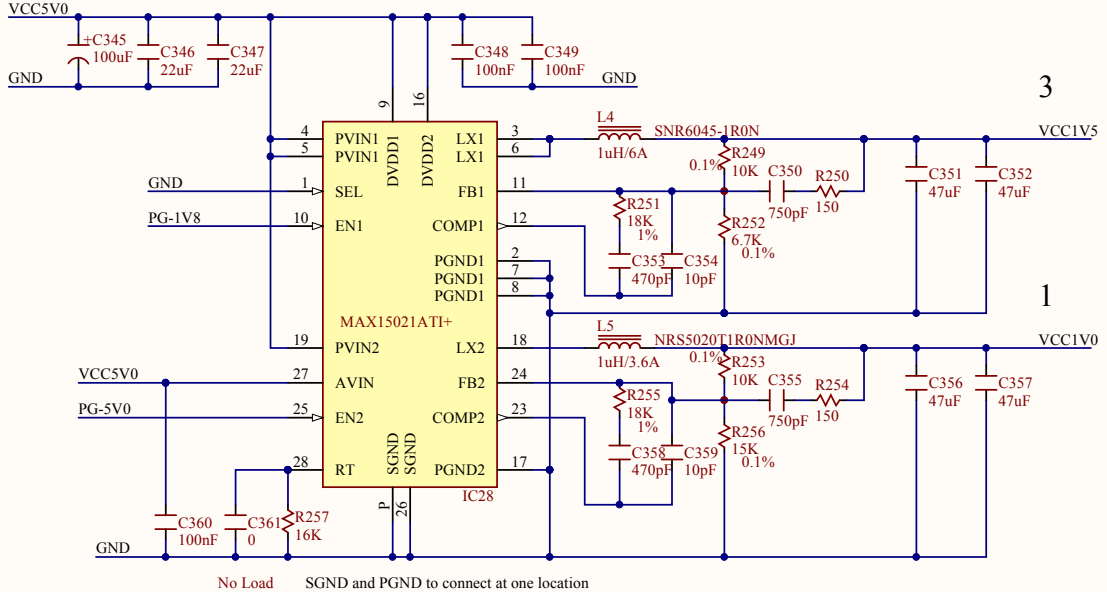
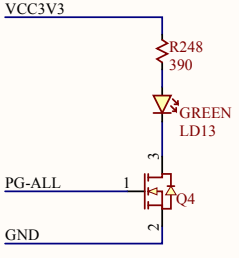



No Load SGND and PGND to connect at one location J18 - 2x2 loaded in 3-6pin location. Pin 1-2 not laoded by default.




No Load SGND and PGND to connect at one location

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|---|---|
| Title | ZED |
| Rev | C.1 |
| Copyright | 2012 |
| Circuit | Power Regulation |
| Doc# | 500-248 |
| Engineer | EG |
| Author | GMA |
| Date | 6/20/2012 |
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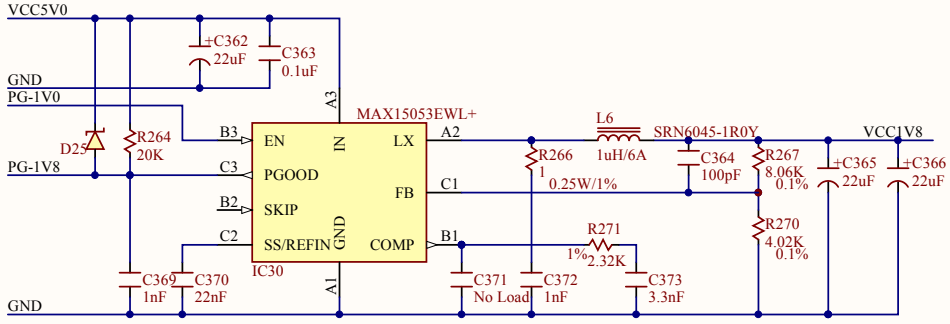


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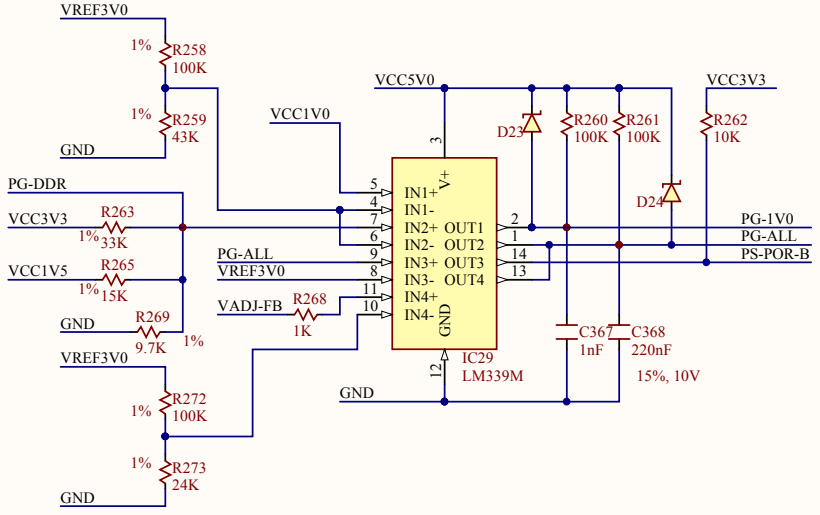


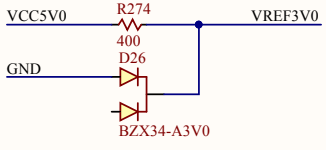


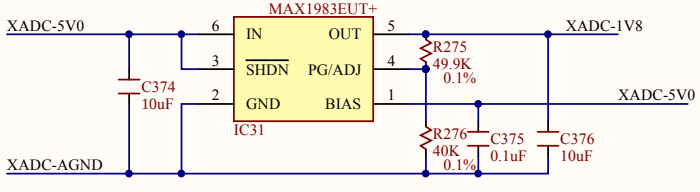


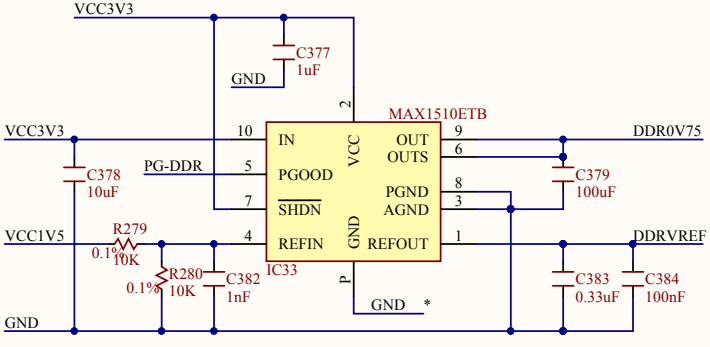


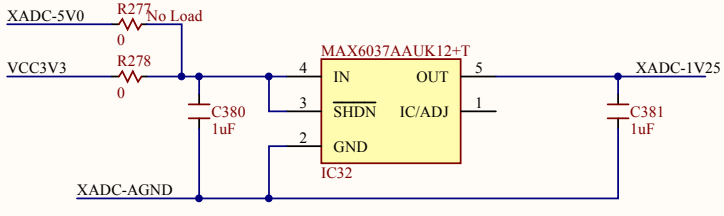


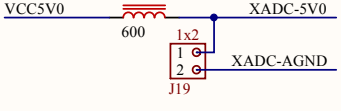


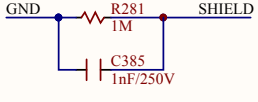


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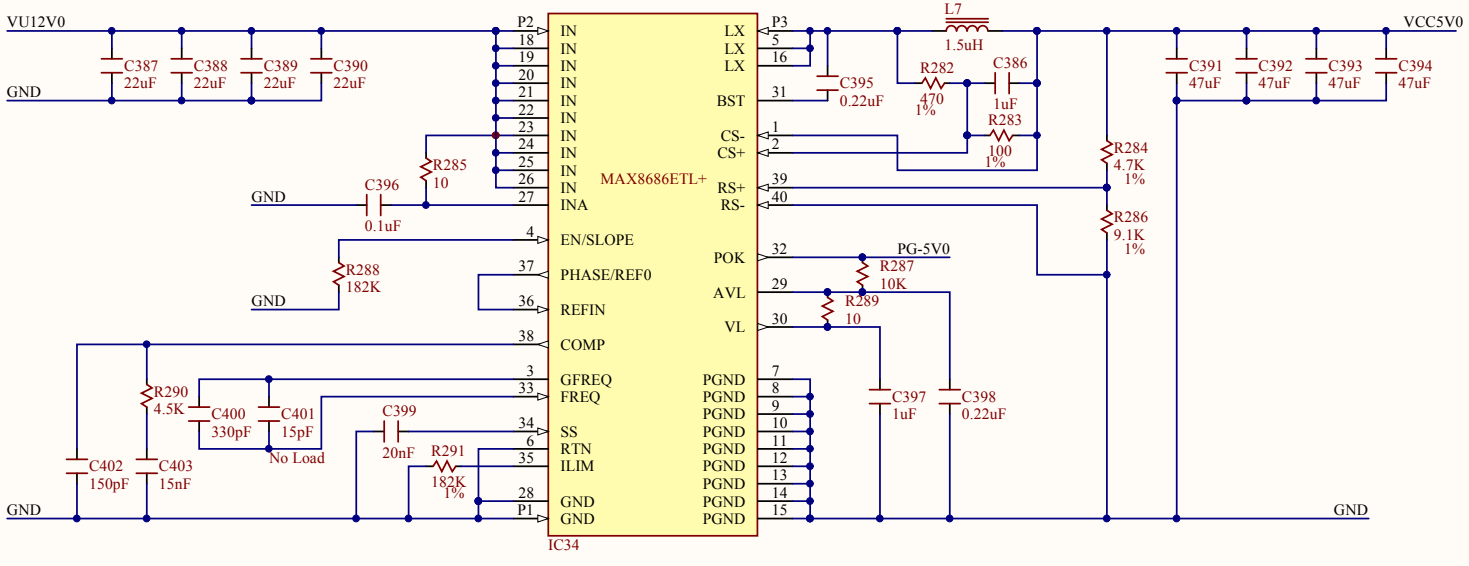


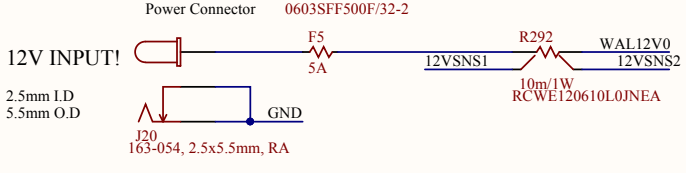


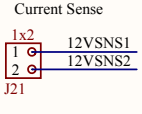


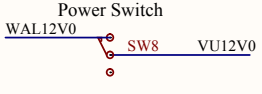


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| Date | 6/20/2012 |
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# Revision History

13 Sep 2012

- Sheet 1: Corrected ZedBoard and Digilent typos
- Sheet 13: Modified IC25, IC26 part number to MT41J128M16HA-15E:D to match BOM
- Sheet 13: Added note regarding new CKE pull-up recommendation
- Sheet 16: Modified C374 capacitor value to be 10uF to match BOM

11 Nov 2012

- Sheet 7: Added note regarding USB-UART VBUS connection, that R150 should be attached to J14.pin1 (V)
- Sheet 8: Added reference to heatsink that is now shipped with ZedBoard
- Sheet 10: Added note regarding new SD-CCLK termination recommendation
- Sheet 13: Added note regarding missing DDR3 symbol pins
- Sheet 13: Added note regarding alternative MT41K128M16JT-125:K DDR3 device

13 Dec 2012

- Sheet 12: Replaced proprietary JTAG circuitry, which cannot duplicated, with a black box for reference and a URL to the module equivalent JTAG-SMT2.

16 Jan 2013

- Sheet 7: Added note regarding TUSB1210 and Zynq timing incompatibility at hot temperature

29 Jan 2013

- Sheet 6: Replaced RJ-45 connector 1840808-7 (obsolete) with replacement 1840750-7